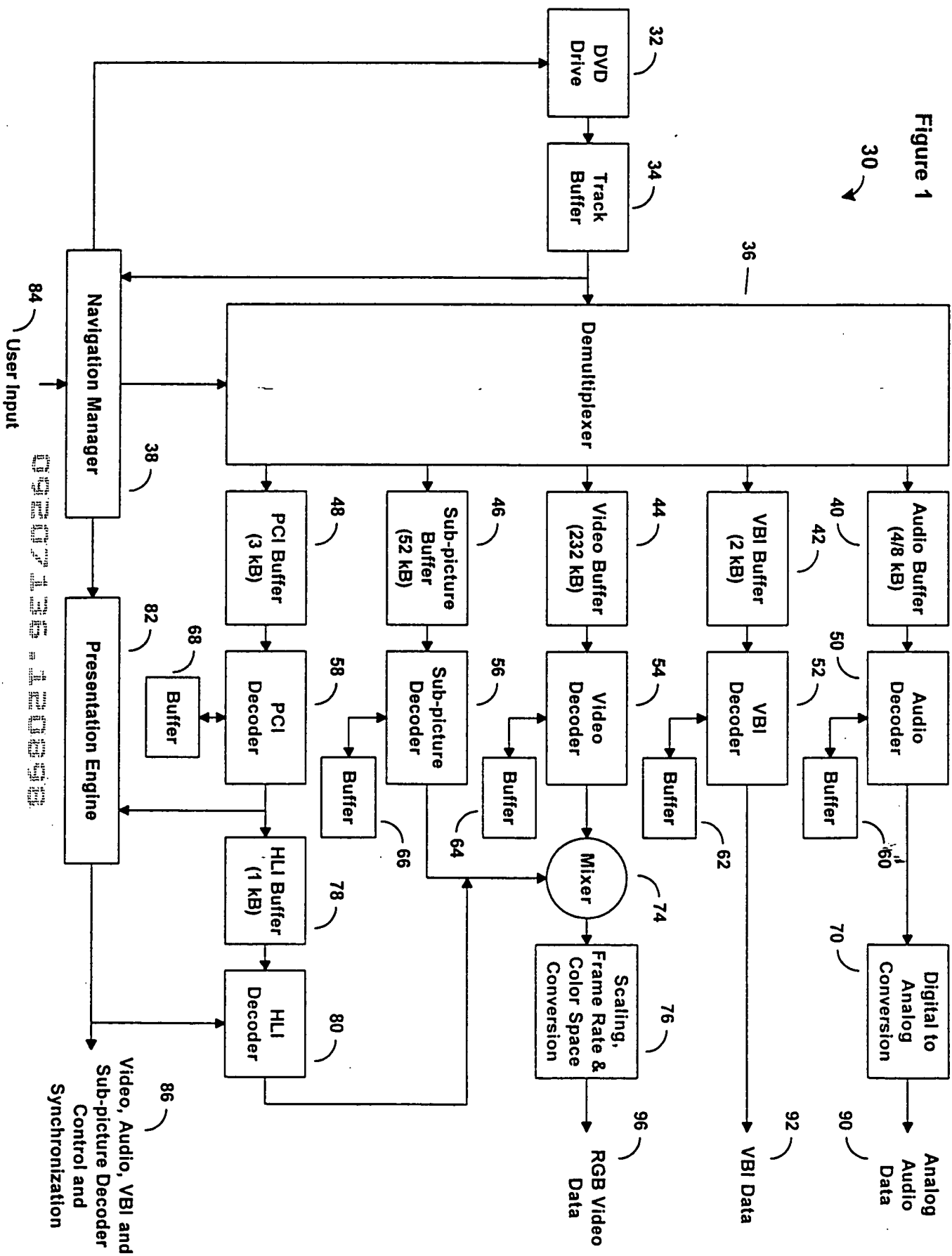


Figure 1



100

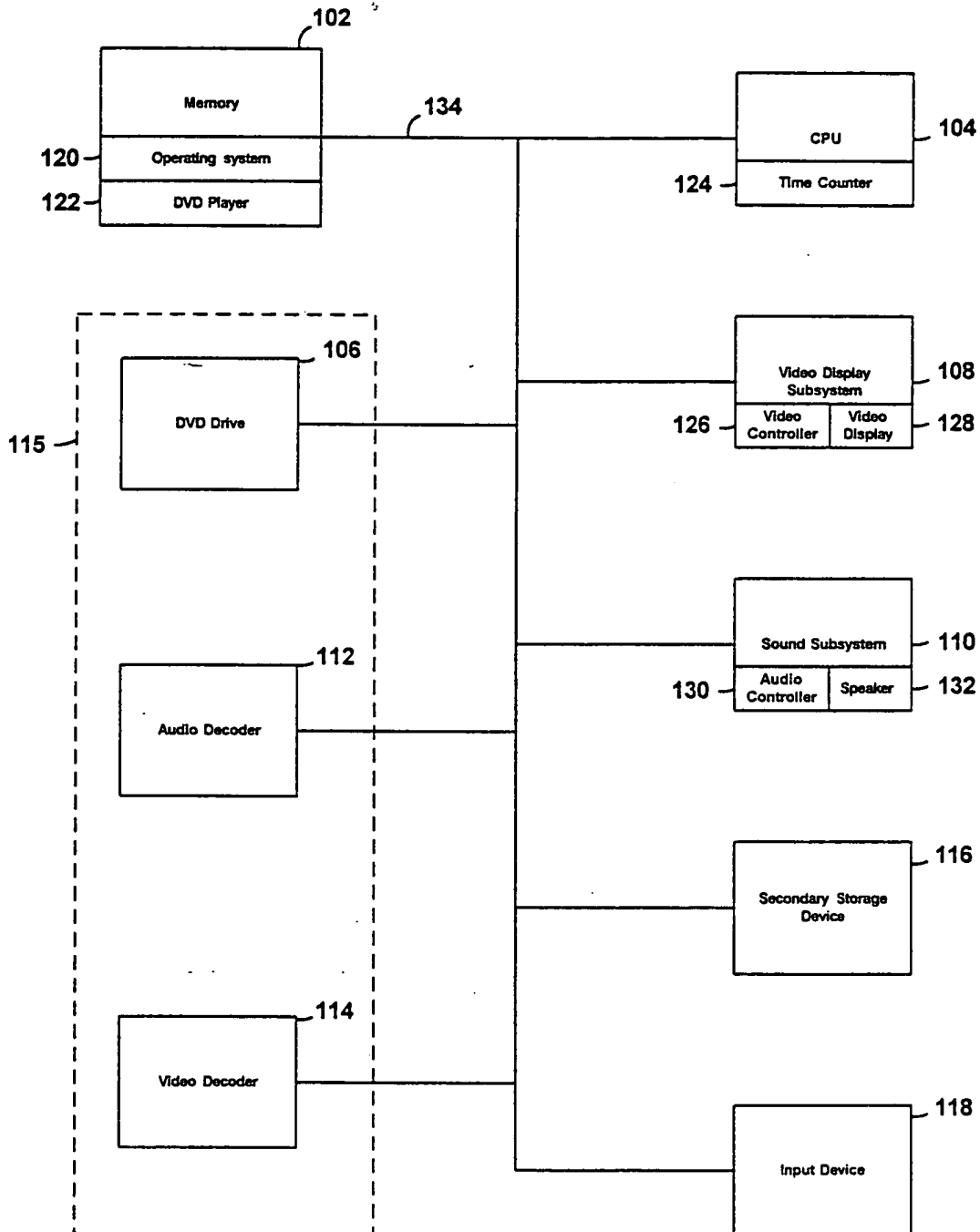


Figure 2

200

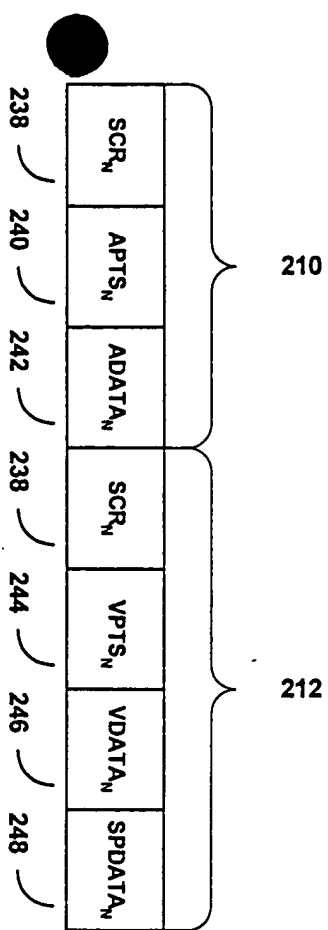
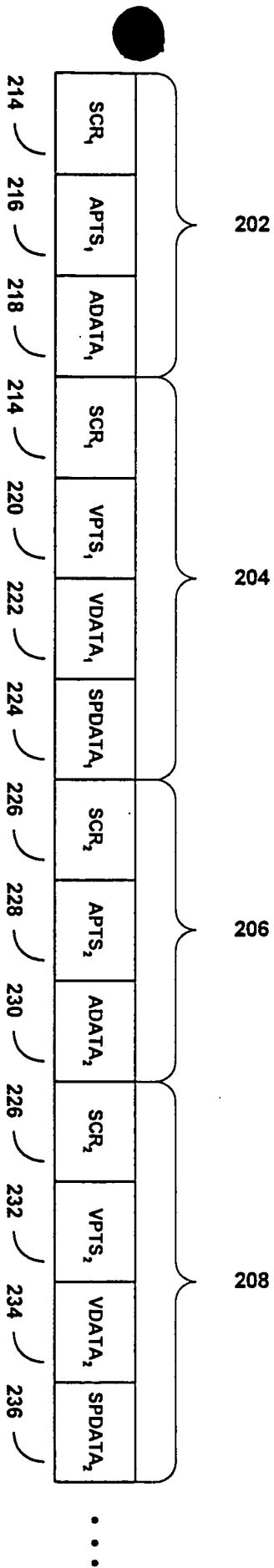


FIGURE 3

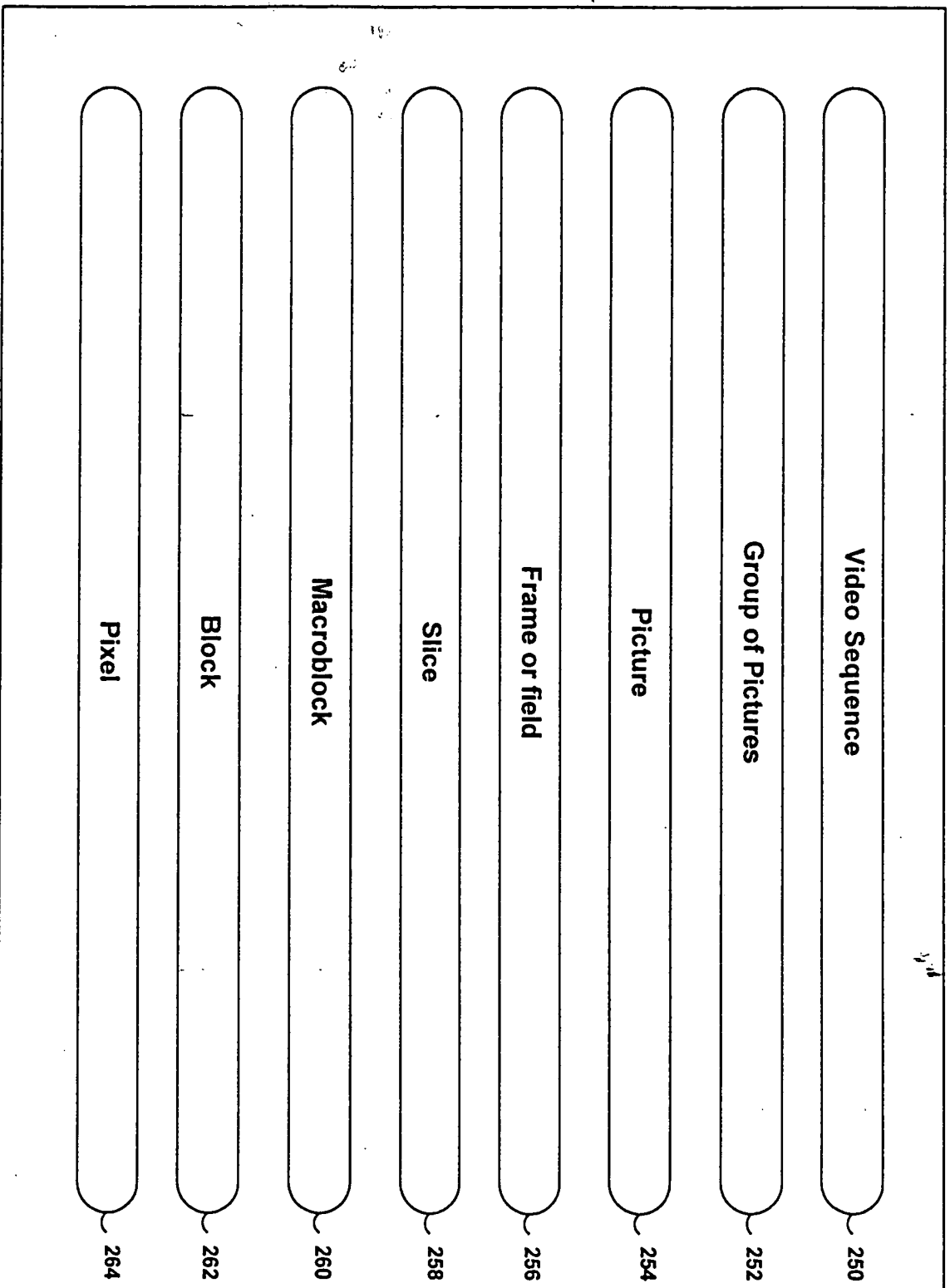


Figure 4

09007130 1200000

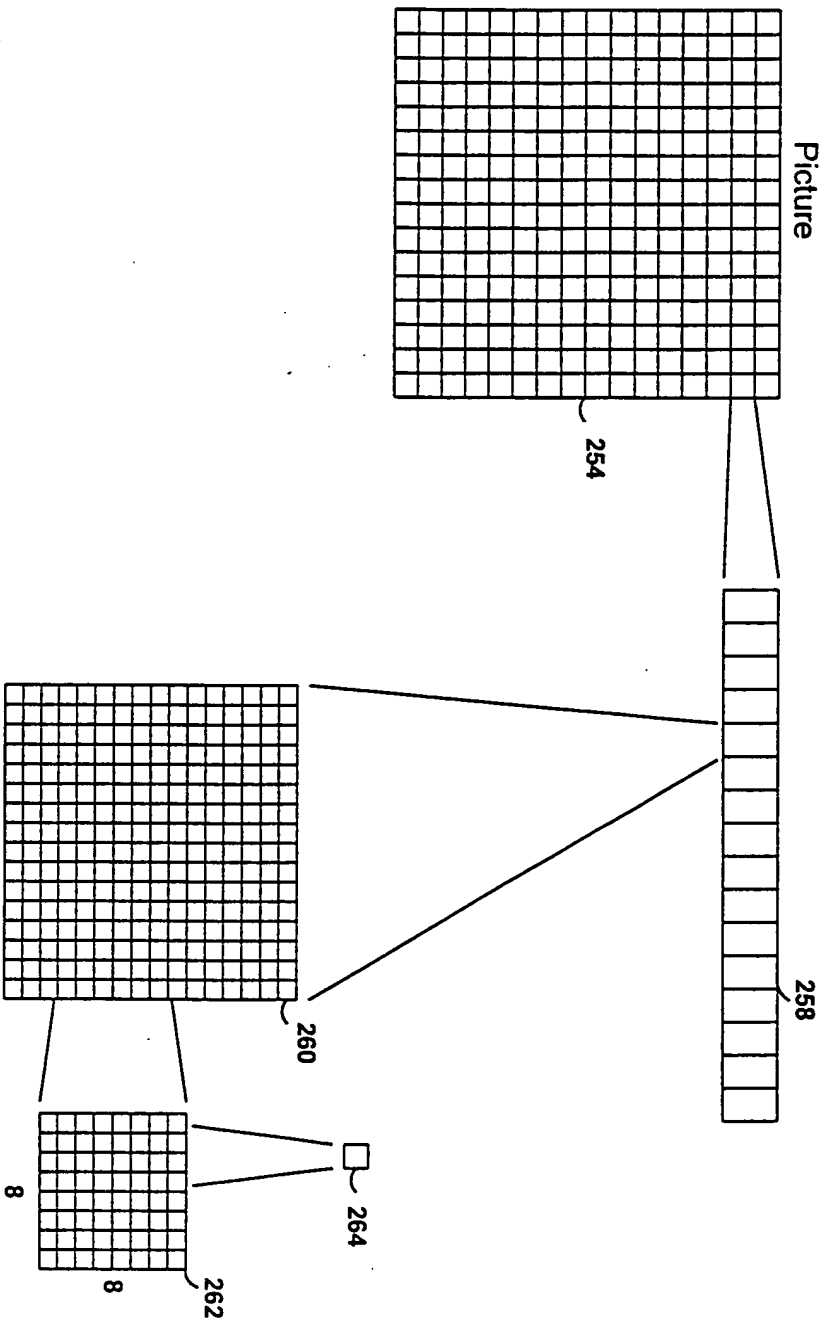


Figure 5

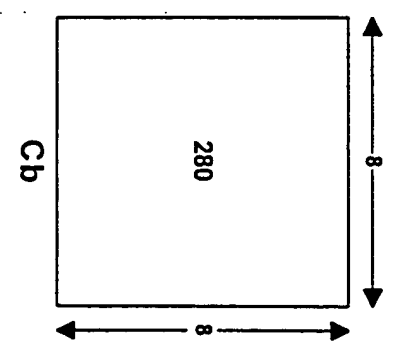
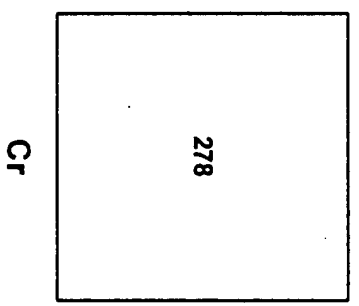
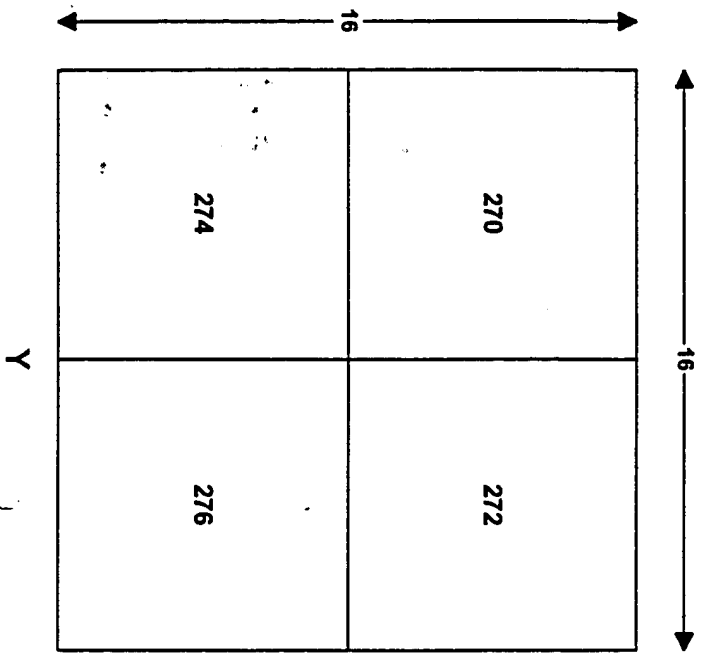


Figure 6

09207435 # 1200993

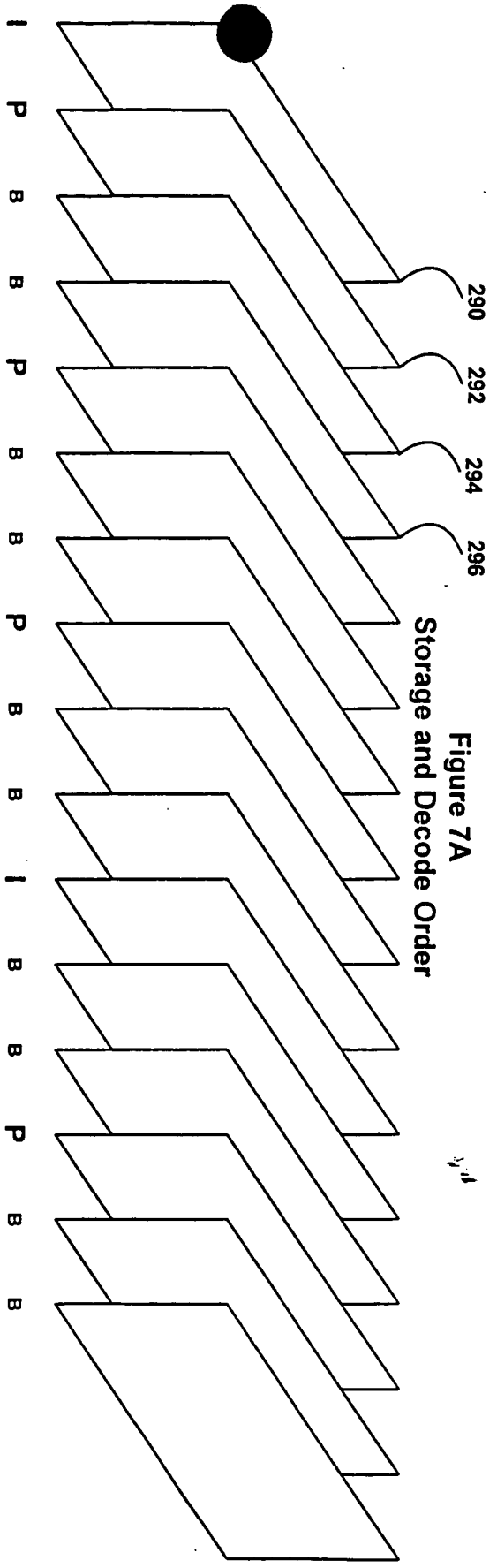


Figure 7A
Storage and Decode Order

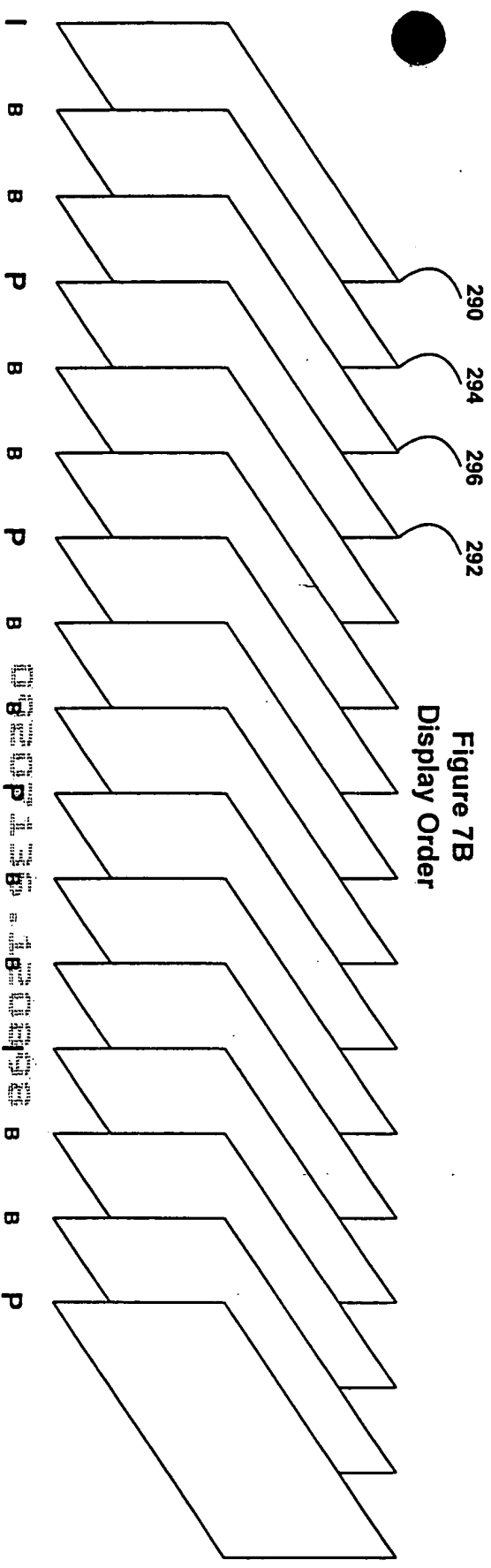


Figure 7B
Display Order

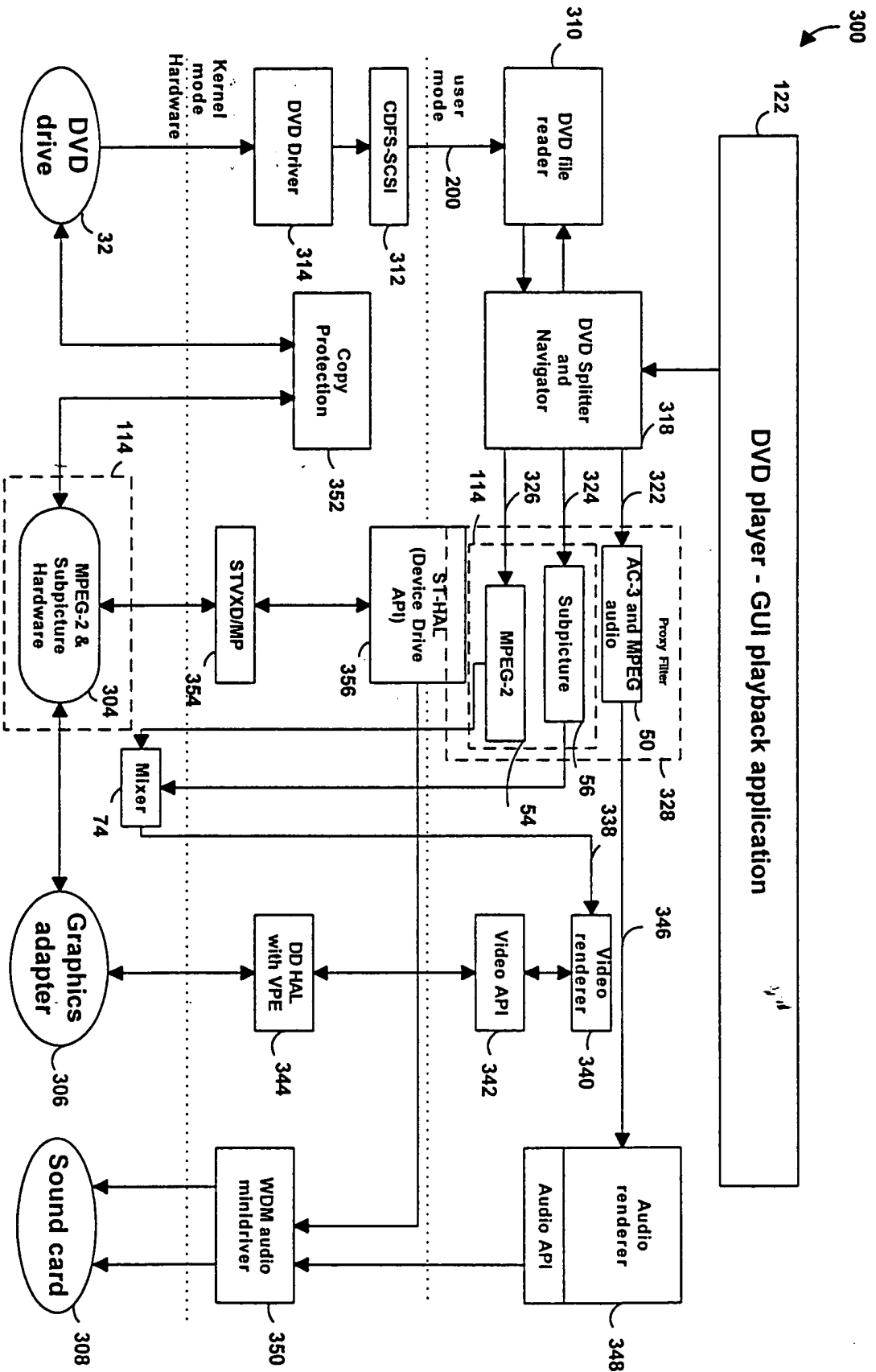


Figure 8

09207139 10000000

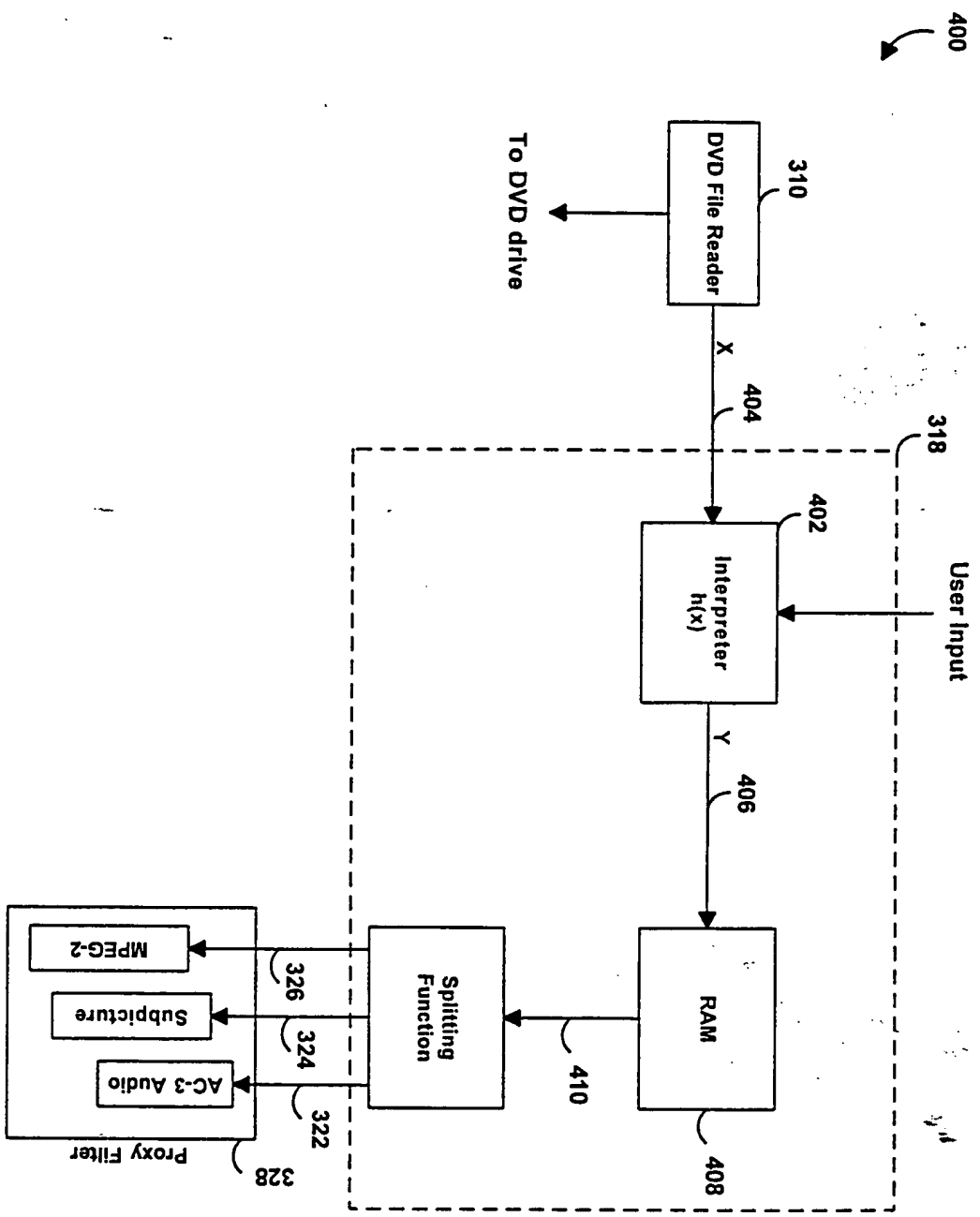


Figure 9

09207135 120298

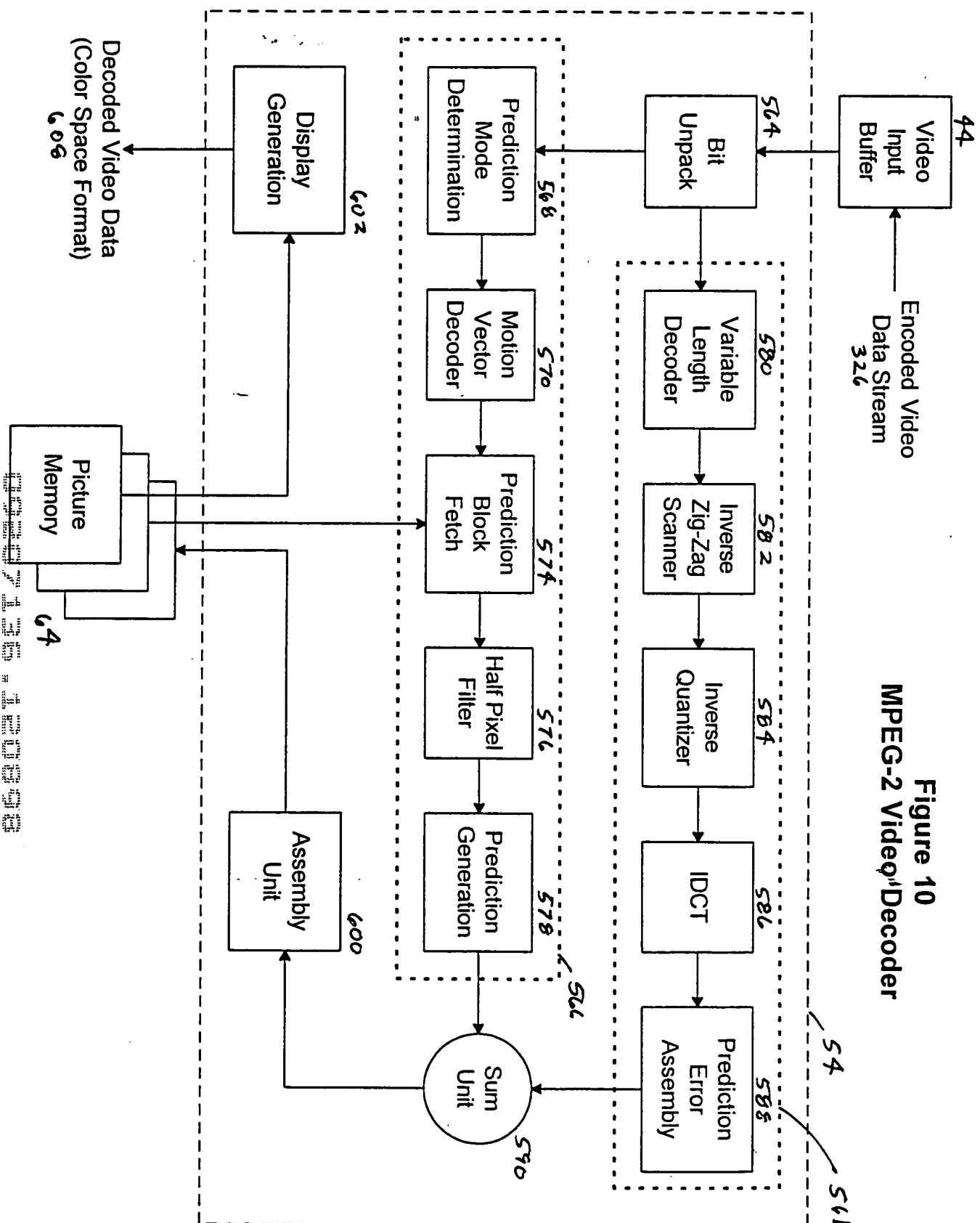
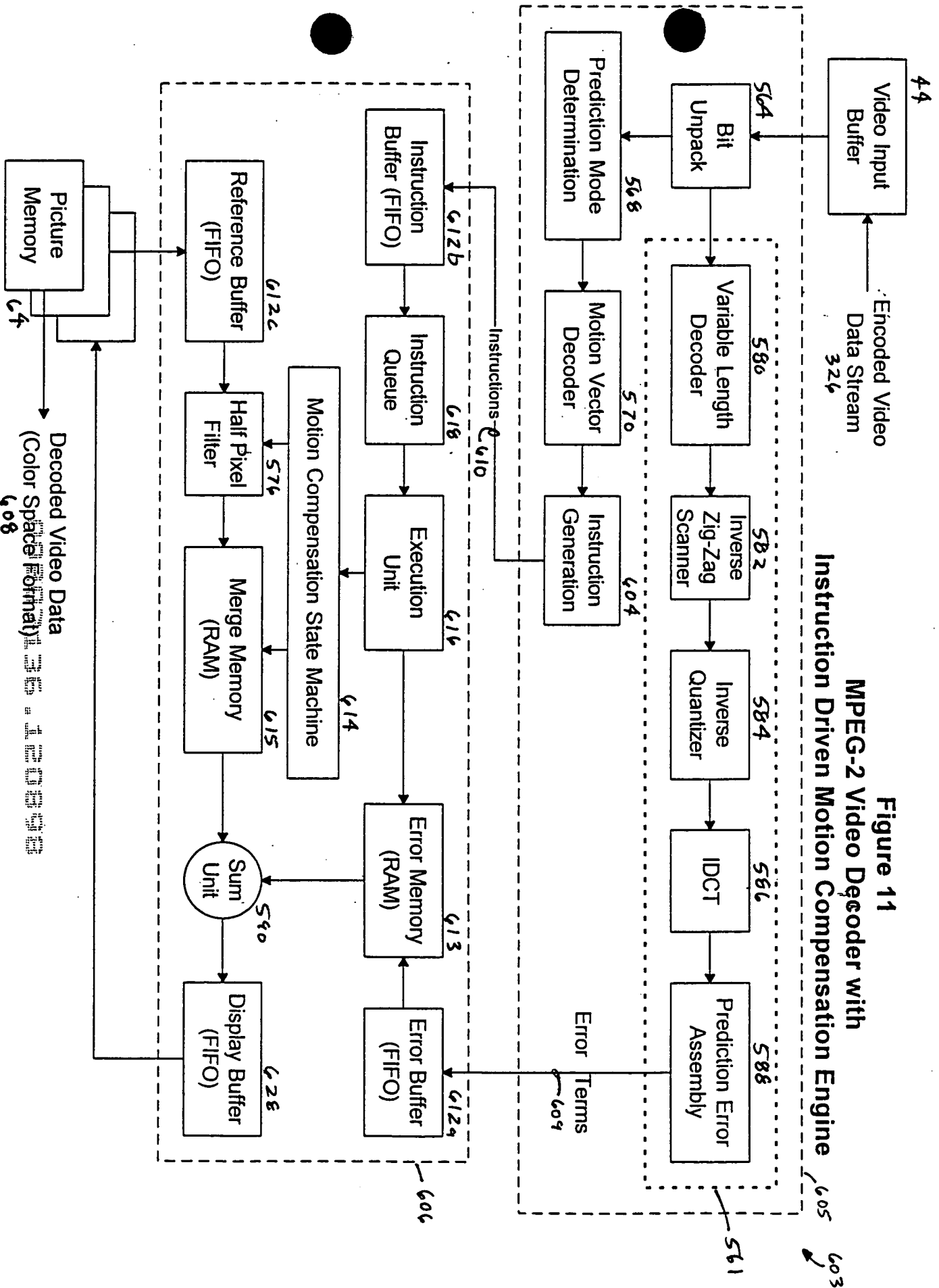


Figure 10
MPEG-2 Video Decoder



Motion Compensation Pipeline Instruction Queue

Load Instructions for 1st Y prediction block in macroblock
Merge Instructions for 2nd Y prediction block in macroblock
:
Merge Instructions for last Y prediction block in macroblock
Write Instructions for predicted Y macroblock
Load Instructions for 1st Cr prediction block in macroblock
Merge Instructions for 2nd Cr prediction block in macroblock
:
Merge Instructions for last Cr prediction block in macroblock
Write Instructions for predicted Cr macroblock
Load Instructions for 1st Cb prediction block in macroblock
Merge Instructions for 2nd Cb prediction block in macroblock
:
Merge Instructions for last Cb prediction block in macroblock
Write Instructions for predicted Cb macroblock
:

Figure 12

Instruction Structure for Predetection Blocks

33	28	27	26	21	20	19	18	17	16	13	12	11	10	8	7	6	5	4	2	1	0
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Figure 13

0907136 130090

Figure 14A
Video Decoder Flowchart
(Prior Art)

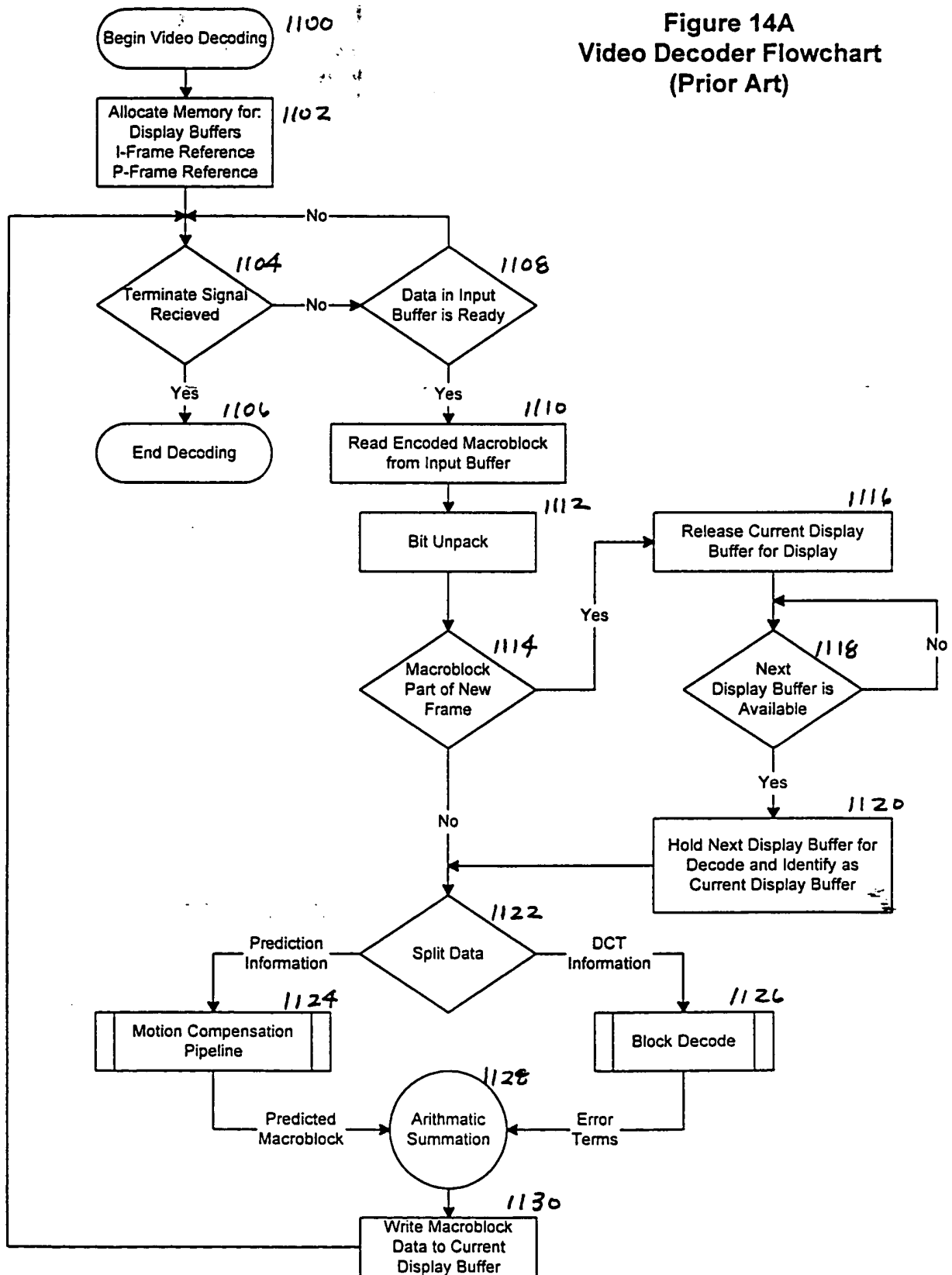


Figure 14B
Motion Compensation
Pipeline Flowchart
(Prior Art)

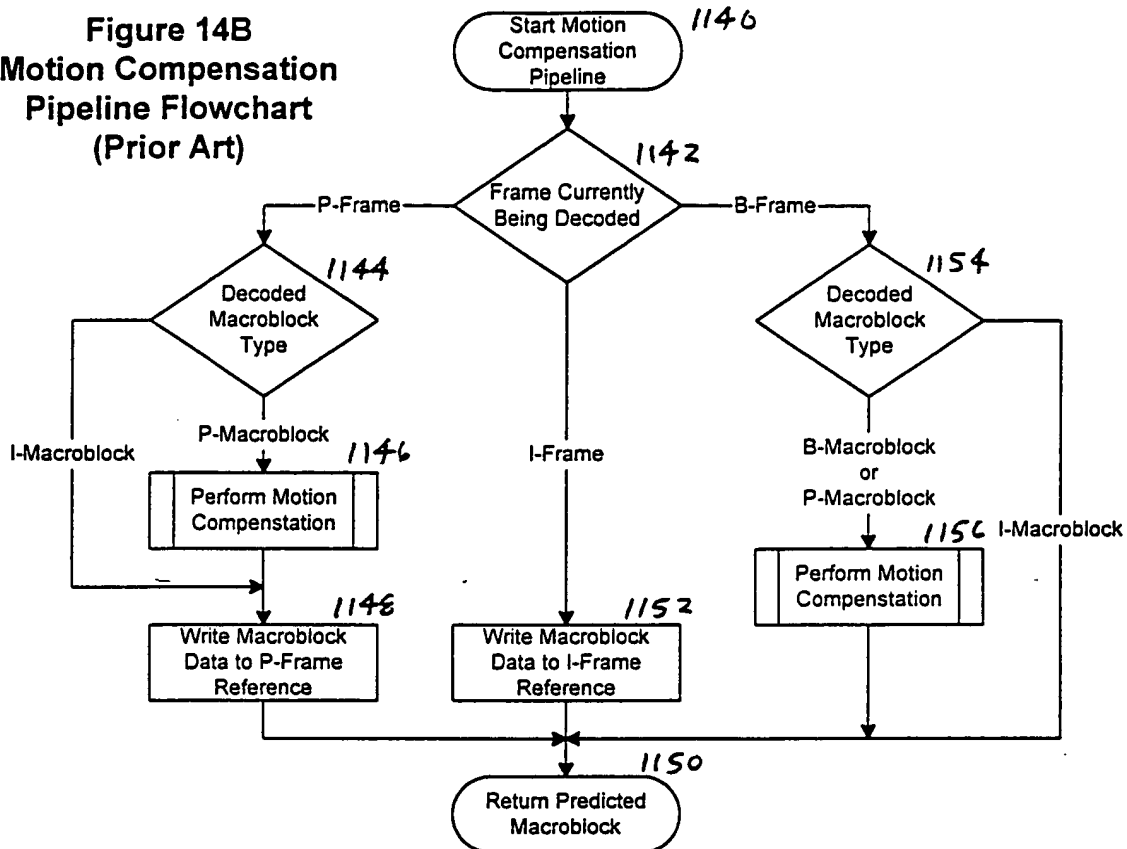


Figure 14C
Block Decode Flowchart
(Prior Art)

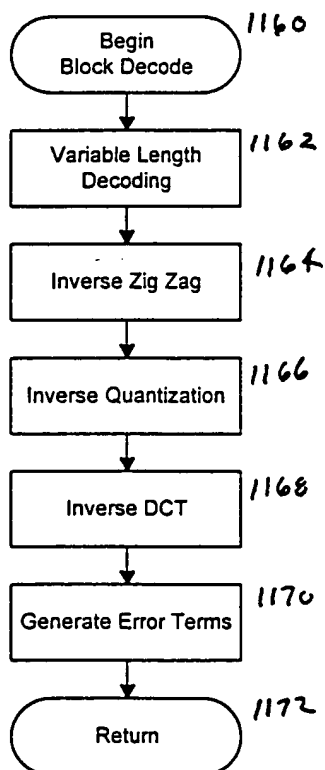


Figure 14D
Perform Compensation Flowchart
(Prior Art)

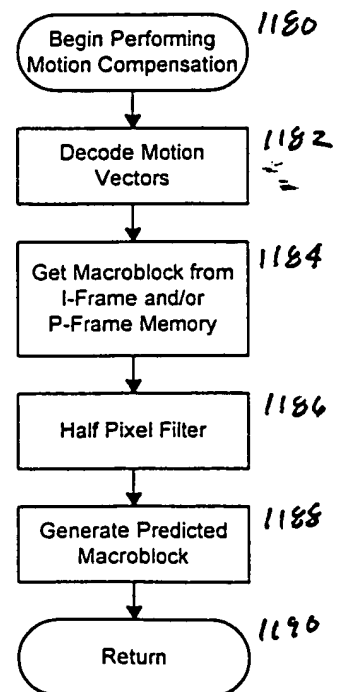


Figure 15A
Video Decoder Flowchart

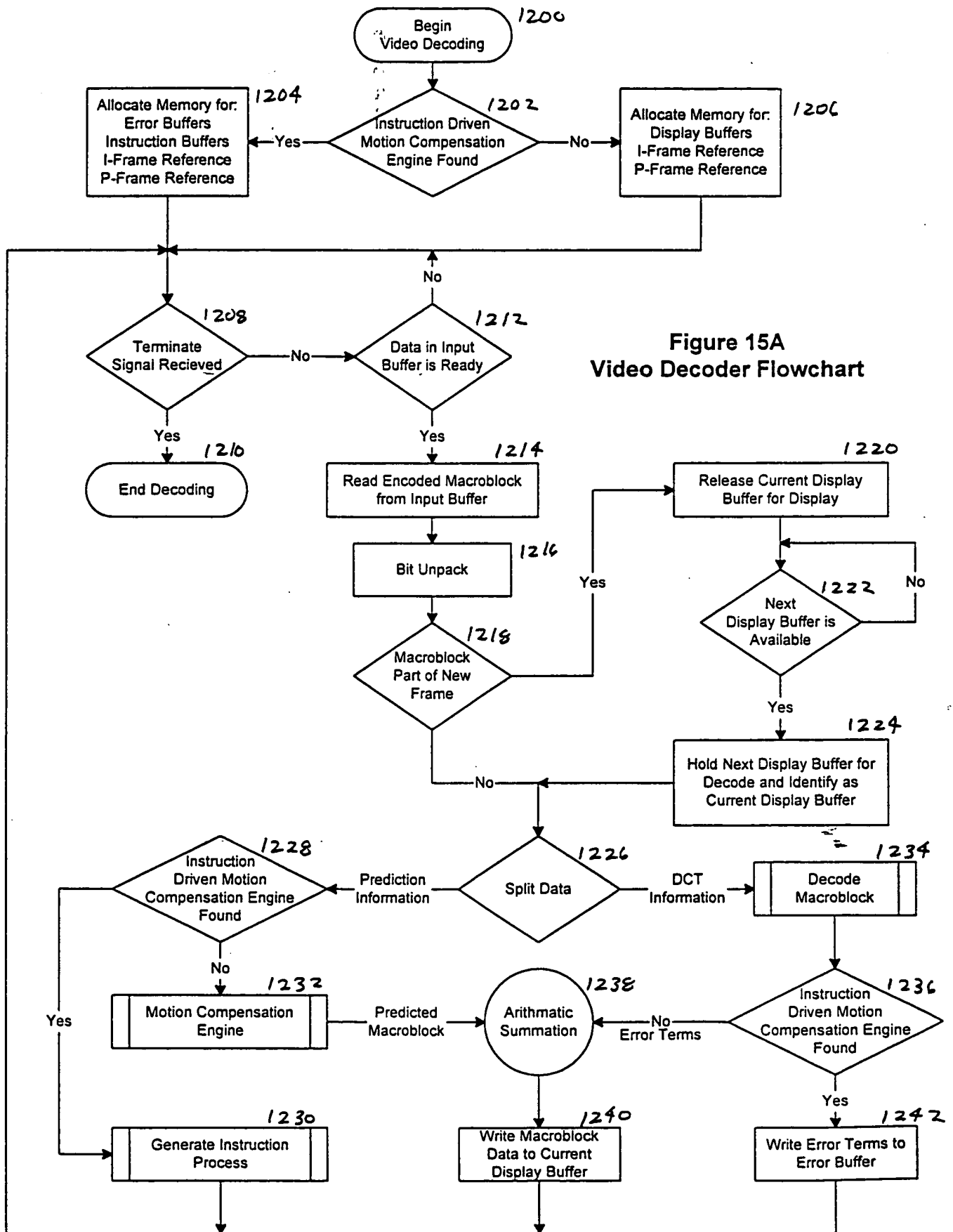
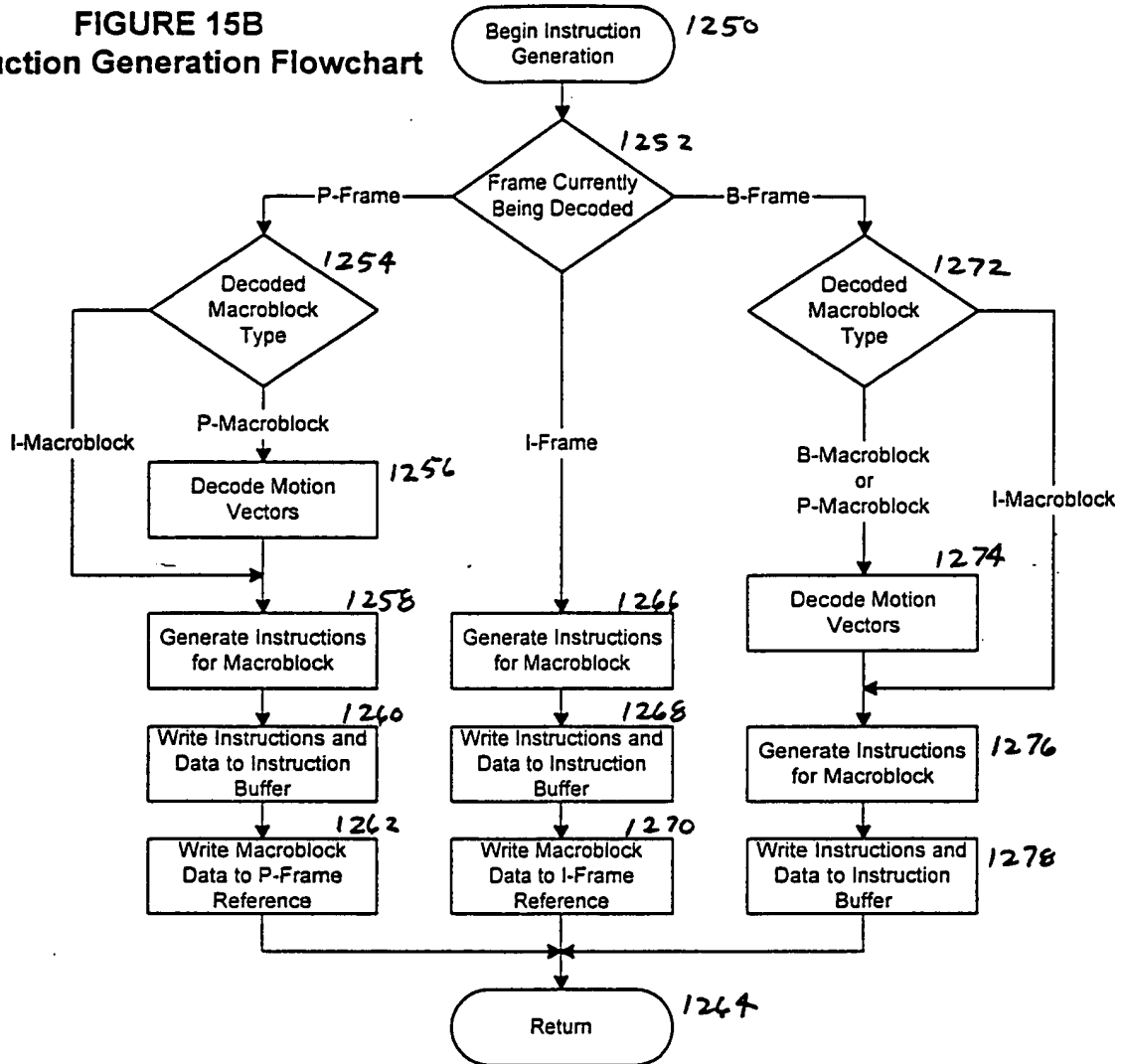


FIGURE 15B
Instruction Generation Flowchart



352027 9470360

Figure 15C
Motion Compensation
Pipeline Flowchart

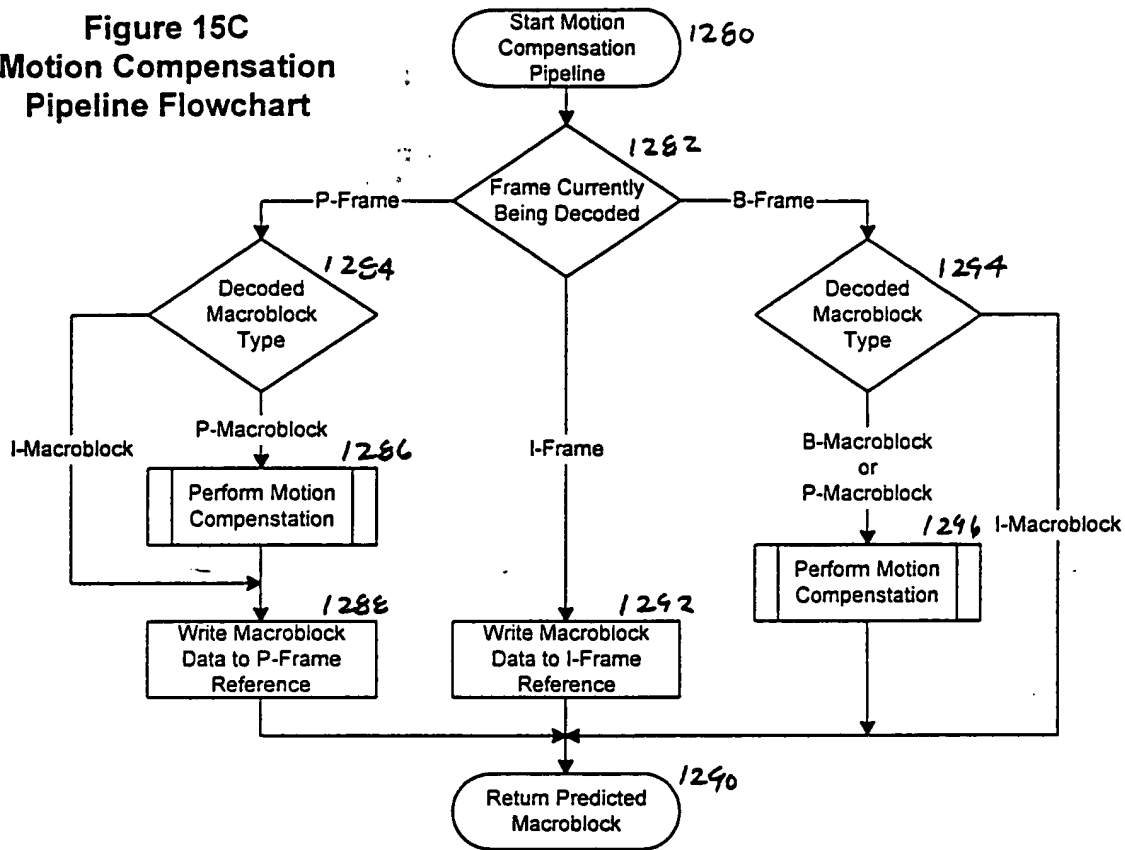


Figure 15D
Block Decode Flowchart

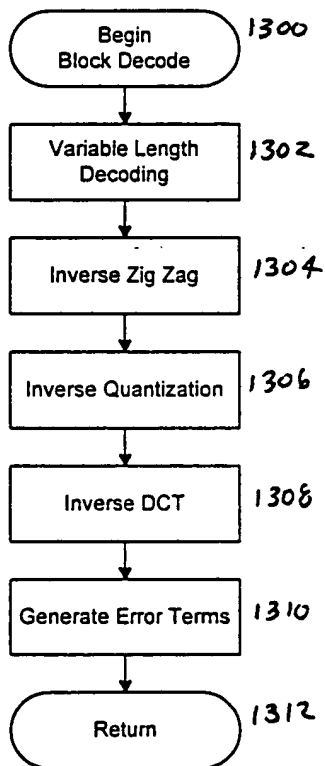
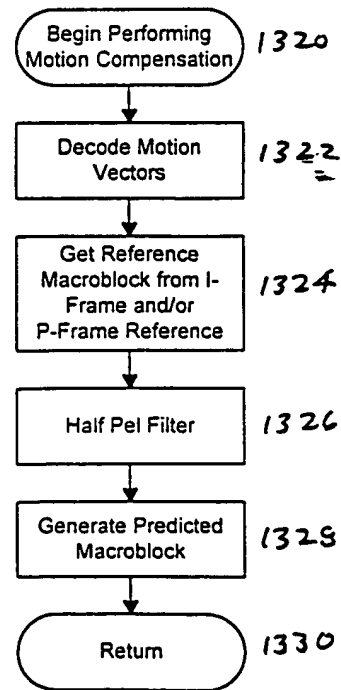


Figure 15E
Perform Motion Compensation
Flowchart



```

graph TD
    1000([Begin Processing]) --> 1002{Instruction in  
Instruction Buffer &  
Instruction Queue  
Not Full}
    1002 -- Yes --> 1004[Read Next Instruction from  
Instruction Buffer]
    1002 -- No --> 1006[Write Instruction to  
Instruction Queue]
    1004 --> 1006
    1006 --> 1008{Instruction in  
Instruction Queue &  
Execution Unit  
Empty}
    1008 -- Yes --> 1010[Read Next Instruction from  
Instruction Queue]
    1008 -- No --> 1012[Write Instruction to  
Execution Unit]
    1010 --> 1012
    1012 --> 1014{Error Term in  
Error Buffer &  
Error Memory  
Not Full}
    1014 -- Yes --> 1016[Read Next Error Term from  
Error Buffer]
    1014 -- No --> 1020{Prediction  
Block in Data  
Buffer & Instruction in  
Execution Unit  
is Load}
    1016 --> 1018[Write Error Term to Error  
Memory]
    1018 --> 1020
    1018 --> 1030{Prediction  
Block in Data  
Buffer & Instruction in  
Execution Unit  
is Merge}
    1020 -- Yes --> 1022[Move the Load Instruction to the  
Motion Compensation State  
Machine]
    1020 -- No --> 1030
    1022 --> 1024[Execute the Load Instruction]
    1030 -- Yes --> 1032[Move the Merge Instruction to the  
Motion Compensation State  
Machine]
    1030 -- No --> 1034{Instruction in  
Execution Unit  
is Write}
    1032 --> 1034
    1034 -- Yes --> 1036[Error Handler]
    1034 -- No --> 1040{Error Memory  
Full}
    1036 --> 1040
    1040 -- Yes --> 1042[Move the Write Instruction to the  
Motion Compensation State  
Machine]
    1040 -- No --> 1036
    1042 --> 1044[Execute the Write Instruction]
    1044 --> 1024
    1024 --> 1026{Terminate  
Processing}
    1026 -- Yes --> 1028([End Processing])
    1026 -- No --> 1002

```

Figure 16A

Figure 16B

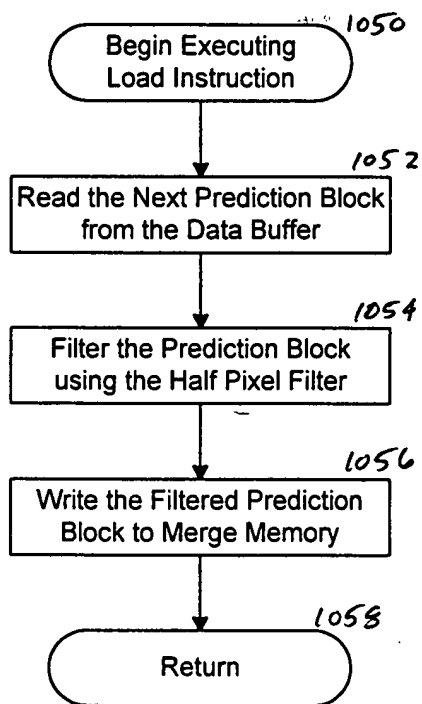


Figure 16C

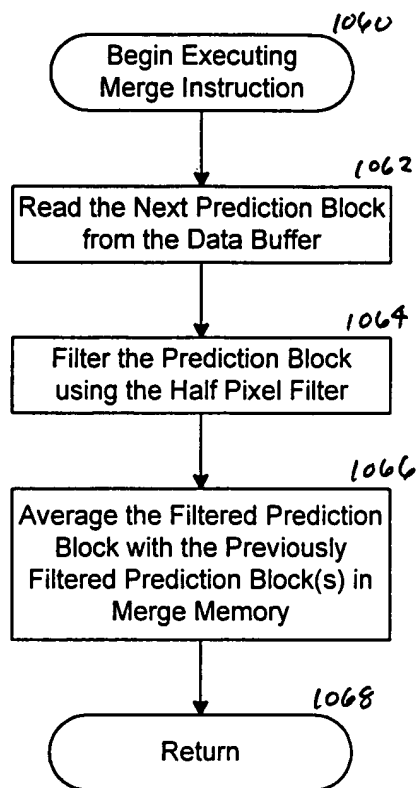
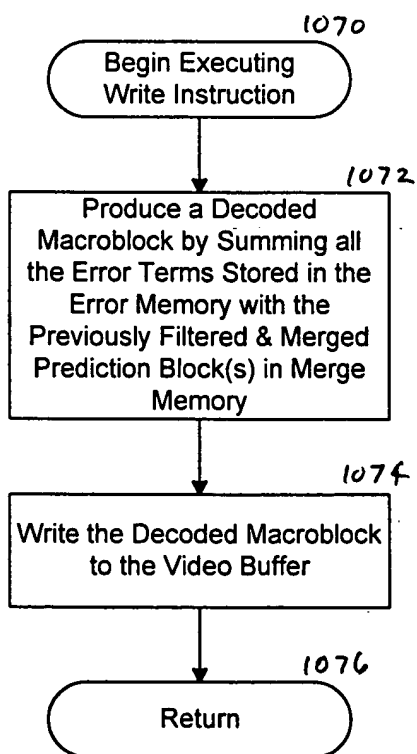


Figure 16D



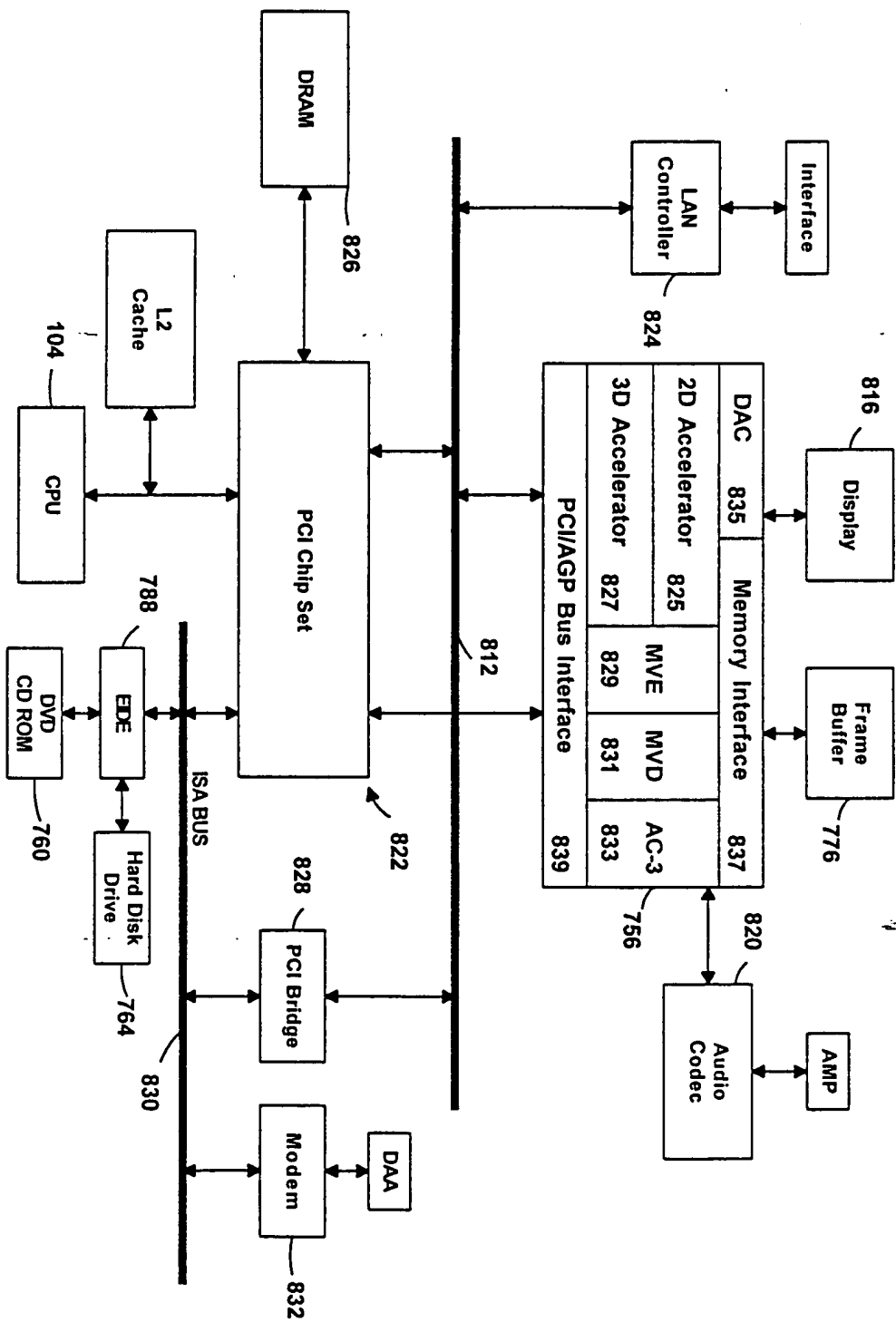


Figure 17

09207135 120893